IN THE MATTER OF German Patent Application
P 17 64 056.1-33
WESTERN ELECTRIC COMPANY

and

IN THE MATTER OF an Opposition thereto by
Siemens AG and AEG-Telefunken

A F F I D A V I T

Gordon E. Moore of 3065 Bowers Avenue, Santa Clara, California 95051, being duly sworn, deposes and says as follows:

I am presently Chairman of the Board of Directors and Chief Executive Officer of Intel Corporation, Santa Clara, California. I received a Bachelor's of Science Degree from the University of California, Berkeley, and a Ph.D Degree in Chemistry and Physics from the California Institute of Technology. I then worked for three years at the Applied Physics Laboratory, Johns Hopkins University, and another year at Shockley Semiconductor Laboratory, Beckman Instruments Corporation. In 1957 I was a cofounder of Fairchild Semiconductor Company where I was Director of Research and Development from 1959 until leaving. I worked there until 1968, at which time I was a cofounder of INTEL Corporation, where I have worked until the present time. I have authored more than 40 technical papers in the field of semiconductor devices and solid state physics. I hold 5 patents in these fields.

In 1967 I was Director of Research and Development at Fairchild Semiconductor. At about that time I heard of a development by R. E. Kerwin and others of Bell Laboratories of a new technique for making MOS devices through the use of a silicon gate electrode. I am not sure who first explained the technique to me, but I believe that it may have been Edward H. Snow, an engineer at Fairchild Semiconductor, who attended an AIME meeting in Boston in 1967, and there heard a description of it by R. E. Kerwin et al.

Upon learning of this silicon gate technique and its advantages, I was convinced that it could be a major advance in MOS integrated circuit technology. This new technique provided gate electrodes which were inherently self-aligned, and it made use of polysilicon electrodes and interconnections which could be subjected to the high temperatures of diffusion treatment. Thus, this technique represented a marked advance over the conventional use of metal gate electrodes and metal interconnections which were not self-aligned with diffusion regions.

I was fully aware of the state of the MOS integrated circuit art at that time, and I was quite surprised to learn that doped polysilicon is satisfactory as a signal conductor in MOS integrated circuits. This is because such circuits are used for digital switching purposes and, if the resistance of the signal conductor is too large, the circuit time constant, which is proportional

to the product of resistance and capacitance, likewise becomes too large, and the switching speed will be reduced. Since reasonably fast switching speed is an important requirement of such circuits, only good conductors can be used. At that time it was thought that only certain metals were sufficiently good conductors. Thus, it was quite surprising and fortuitous that polysilicon could be used as a conductor because it is compatible with the other materials of the integrated circuit, it is capable of withstanding high temperature treatment, and it can be converted to highly insulative silicon dioxide, among other advantages.

In 1968, along with Dr. Robert Noyce, I founded INTEL Corporation. We believed that the fabrication of semiconductor memory chips making use of silicon gate technology represented an opportunity which justified the risk of starting a new business.

Our new company was able to make and sell silicon gate integrated circuits, and our early experience is set forth in a paper which I coauthored, "Silicon Gate Technology", L. L. Vadasz et al, "IEEE Spectrum" October, 1969 pages 28-35, a copy of which is attached hereto as exhibit C. The section on page 31 entitled, "Reducing Parasitics" sets forth the advantages of the self-aligned silicon gate and the section on pages 31-33 entitled, "High Functional Density" sets forth in detail the advantages of polysilicon interconnections. Our initial estimate of silicon gate technology was fully justified and our company prospered. In 1969 INTEL sales of integrated

circuits using silicon gate technology was $600,000, and in 1979 INTEL sales of devices of this type was hundreds of millions of dollars which demonstrates the dramatic commercial success for INTEL of this product. INTEL'S production of integrated circuits using silicon gate technology is, of course, only a fraction of the total world-wide production.

It has always been my understanding that the silicon gate technique originated with R. E. Kerwin et al of Bell Laboratories. Recognition by the scientific community of important contributions is conventionally made by making reference in published papers to such contributions. Thus, in my published paper which constitutes exhibit C, the first reference is to the published paper of R. E. Kerwin et al describing the silicon gate technique.

It is my understanding that the scientific community in general has likewise attributed that contribution to R. E. Kerwin et al.

Our choice of the silicon gate technique of R. E. Kerwin et al was an important part of INTEL'S strategy when the company was started in 1968, and it has subsequently been largely responsible for INTEL'S growth and success.

Gordon E. Moore

State of California)
County of Santa Clara)

Sworn to and subscribed before me this 7 day of July 1980.

Jean C. Jones
Notary Public

OFFICIAL SEAL
JEAN C. JONES
NOTARY PUBLIC — CALIFORNIA
PRINCIPAL OFFICE IN THE
COUNTY OF SANTA CLARA
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